REMARKS

Claims 1-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over D'Amico et al. (U.S. Patent Application Publication Number 2004/0001477, hereinafter "'477"). Respectfully disagreeing with these rejections, reconsideration is requested by the applicants. Nonetheless, claims 14-17 have been canceled.

Regarding independent claims 1 and 10, '477 paragraphs [0014, 0020, and 0026] are cited as teaching the claim language. '477 [0014] reads:

> [0014] Turning now to FIG. 1, a block diagram of a transmitter and receiver pair used in a CDMA VOIP system with associated buffers consistent with certain embodiments of the present invention is illustrated. In a two-way communication VOIP CDMA system, a transmitter and a receiver is present at each end, but for simplification, consider only a single transmitting and receiving pair for now. Transmitter 104 incorporates a buffer 108 with a variable delay designated D1 in the digital signal path that is controlled in a manner as will be described later. This buffer 108 can be at any suitable location within the digital signal path prior to wireless transmission over a VOIP air interface 112. At the receiver end, a receiver 116 incorporates a second buffer 120 that has a variable associated delay designated D2.

'477 [0020] reads (emphasis added):

> [0020] FIG. 2 illustrates a method 200 for monitoring and adjusting the soft capacity of the system to accommodate instantaneous excess packet transmission needs starting at 202. **This method assumes that the status of D2 buffers 120 is tracked (or alternatively fed back) and analyzed at the associated transmitter 104. Transmitter 104, using internal processing capabilities, then determines at 206 if there are any D2 buffers 120 that are near zero delay.** Near zero can be defined as a delay less than a predetermined threshold, e.g. 5 ms in the current example. If not, no action is taken. If so, a determination is made as to whether the delays are due to congestion at 210. If not, no action is taken. If so, a determination is made as to whether a slight temporary degradation of S/I+ N is acceptable to overcome the current congestion. If not, no action is taken. **If so, the associated packets are sent** to prevent D2 buffer 120 under-runs at 218. Control then returns to 206 and the status of the D2 buffers 120 is continuously monitored to determine the need for adjustment in the soft capacity of the system. This method can be used in conjunction with other methods that do not impact the overall system's performance and can thus be balanced using prioritization arrangement in conjunction with other techniques.

'477 [0026] reads:

> [0026] Turning now to FIG. 6, a more detailed block diagram of a transceiver pair used in a CDMA VOIP system with associated buffers consistent with certain embodiments of the present invention is illustrated. In a two-way communication VOIP CDMA system, a transmitter and a receiver is present at each end. This is illustrated in a transceiver 604 coupled to transceiver 616. Transceiver 604 (operating as the transmitting side) incorporates a transmitter 606 and a receiver 610. (Note that the voice buffer and other blocks associated with receiver 610 are not shown in the diagram for simplicity.) Transceiver 604 also incorporates buffer 108 with a variable delay designated D1 in the digital signal path that is controlled by a control processor 620. This buffer 108 receives VOIP format packets of voice from vocoder 624. Vocoder 624 operates with its rate controlled by processor 620. In accordance with one embodiment consistent with the present invention, processor 620 encodes the first packet of an utterance with an indication of the delay D1 of buffer 108 and that packet is transmitted along with the other packets making up the utterance over the VOIP air interface 112 to transceiver 616. Control processor 620 receives input regarding (or alternatively tracks) the D2 buffer states of transceiver 616 as well as other receivers, information regarding network congestion, link quality information, real- time and non-real time traffic information and overall system C/N+I information. The control processor 620 is also programmed with short-term network capacity targets and other information.

The passages of '477 cited by the Examiner above clearly discloses that the **transmit-side determines whether any D2 buffers are near zero delay**. To do this, it is assumed that the status of the D2 buffers are tracked (or alternatively fed back). In contrast, the present claims recite (claim 1 language, e.g.) sending an indication to the source mobile unit when the remaining play-out depth of the play-out buffer in the destination mobile unit reaches a predetermined threshold. Thus, as claimed, the **transmit-side is sent an indication when a predetermined threshold is reached in the receive-side play-out buffer.**

The applicants submit that '477 does not teach or suggest this claimed operation. In particular, claim 1 recites (emphasis added) "sending an indication to the source mobile unit **when the remaining play-out depth of the play-out buffer in the destination mobile unit reaches a predetermined threshold.**" Claim 10 recites (emphasis added), "A system comprising...a **destination mobile unit**...receiving the voice communications from the infrastructure, the destination mobile unit **comprising a play-out buffer, the play-out buffer having an associated play-out depth**, the

destination wireless unit storing the voice communications in the play-out buffer and **forming an indication when the play-out depth reaches a predetermined threshold."**

Regarding claims 2, 6 and 18, '477 [0020, 0026 and 0027] are cited as teaching much of the claim language. '477 [0026 and 0027] reads (emphasis added):

> [0026] Turning now to FIG. 6, a more detailed block diagram of a transceiver pair used in a CDMA VOIP system with associated buffers consistent with certain embodiments of the present invention is illustrated. In a two-way communication VOIP CDMA system, a transmitter and a receiver is present at each end. This is illustrated in a transceiver 604 coupled to transceiver 616. Transceiver 604 (operating as the transmitting side) incorporates a transmitter 606 and a receiver 610. (Note that the voice buffer and other blocks associated with receiver 610 are not shown in the diagram for simplicity.) Transceiver 604 also incorporates buffer 108 with a variable delay designated D1 in the digital signal path that is controlled by a control processor 620. This buffer 108 receives VOIP format packets of voice from vocoder 624. **Vocoder 624 operates with its rate controlled by processor 620.** In accordance with one embodiment consistent with the present invention, processor 620 encodes the first packet of an utterance with an indication of the delay D1 of buffer 108 and that packet is transmitted along with the other packets making up the utterance over the VOIP air interface 112 to transceiver 616. Control processor 620 receives input regarding (or alternatively tracks) the D2 buffer states of transceiver 616 as well as other receivers, information regarding network congestion, link quality information, real- time and non-real time traffic information and overall system C/N+I information. The control processor 620 is also programmed with short-term network capacity targets and other information.
>
> [0027] At the transceiver 616 (illustrated operating as the receiver side), a receiver 630 is coupled to buffer 120 that has variable delay D2. **The state of the link quality, status of D2 and other information can be fed back to transceiver 604 via transmitter 636 through air interface 112 to receiver 610.** (Note again that the voice buffer and other blocks associated with transmitter 636 are not shown for simplicity.) A control processor 650 at transceiver 616 operates in a manner similar to that of processor 620 in transmission mode and in receive mode receives the first packet in an utterance, decodes the value of D1 and calculates the amount of initial delay required to maintain a fixed delay for D1+D2. Alternatively, control processor 620 can make that calculation and transmit the initial value of D2 along with the first packet in an utterance (either as part of that packet or as a separate control packet).

The passages of '477 cited by the Examiner above (i.e., [0020, 0026 and 0027]) describe a vocoder with its rate controlled by a processor ([0026]) and sending **packets** to prevent D2 buffer under-runs when the proper conditions are met ([0020]). In contrast, the claims recite (emphasis added) **"adjusting the coding rate** of the

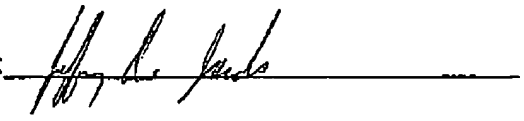
communications sent from the source mobile unit to the destination mobile unit **as a function, at least in part, of the indication received from the destination mobile unit**" (claim 2), "**adjusting the coding rate of the vocoder** in the source mobile unit **according to the indication received from the destination mobile unit**" (claim 6), and "a **vocoder** having a communication output and a control input and further having an associated **adjustable vocoder coding rate that is responsive to the control input**; and a controller that is operably coupled to the storage register and coupled to the vocoder by the control input, the controller **forming a signal on the control input based upon contents of the at least one indication message** present in the storage register" (claim 18).

In the Examiner's *Response to Arguments* section of the present office action, the Examiner also refers to claim 2 of '477, which recites (emphasis added) "a vocoder that digitally encodes speech signals at a specified vocoder rate; and means for adjusting the vocoder rate **based upon a measure of traffic loading of the wireless network.**" The applicants recognize that changing a vocoder's rate is well-known; however, the applicants submit that not all of the the reasons for changing a vocoder rate or for determining / re-determining a vocoder's rate are known. As cited by the Examiner, '477 teaches adjusting the vocoder rate based upon a measure of traffic loading of the wireless network. The applicants submit that what is claimed (see the quotes above) is different and not suggested by '477.

Since none of the references cited, either independently or in combination, teach all of the limitations of independent claims 1, 6, 10 or 18, or therefore, all the limitations of their respective dependent claims, it is asserted that neither anticipation nor a prima facie case for obviousness has been shown. No remaining grounds for rejection or objection being given, the claims in their present form are asserted to be patentable over the prior art of record and in condition for allowance. Therefore, allowance and issuance of this case is earnestly solicited.

The Examiner is invited to contact the undersigned, if such communication would advance the prosecution of the present application. Lastly, please charge any additional fees (including extension of time fees) or credit overpayment to Deposit Account No. **502117 – Motorola, Inc.**

Respectfully submitted,
J. Harris et al.

By: 

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